Docket No.: 59472-8025.US01
SIMG-0091

(PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:
OOK KIM ET AL.

Examiner: Brooke J. Dews

Application No.: 10/658,590

Confirmation No.: 1927

Filed: SEPTEMBER 8, 2003

Art Unit: 2182

For: METHOD AND APPARATUS FOR ENCODING AND COUPLING CONTROL SIGNALS ONTO A COMMON BUS A PLURALITY OF PARALLEL AND SERIAL DISK DRIVES THAT CARRIES SIGNALS AT DOUBLE A BASE DATA RATE (AS AMENDED)

DECLARATION OF PRIOR INVENTION BY OOK KIM UNDER 37 C.F.R. § 1.131

MS Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

I, **Ook Kim**, declare and state that:

1. I am a joint inventor, along with Sungjoon Kim, Robert Norman, Chi Wai Ho, Frank Lee, Dongyun Lee, Gijung Ahn, and Seung Ho Hwang, of the invention described and claimed in U.S. Patent Application No. 10/658,590 (the "Present Application"), filed on 08 September 2003.

2. I am also an inventor, and contributed to the subject matter described in U.S. Provisional Patent Application No. 60/409,367 (the "Provisional Application"), filed on 06 September 2002, to which the Present Application claims the benefit of priority date.

3. This Declaration establishes invention in this country of the subject matter in the currently pending claims in the Present Application before the effective

reference date and corresponding to the actual filing date of U.S. Patent Publication No. 2003/0191872 filed on 27 June 2002 by Frank Barth ("Barth").

4. All of the work described within this Declaration was performed in the United States, by me or by my joint inventors, or on my behalf and under my direction.

5. I have reviewed my invention proposal disclosure records, including the Exhibit A submitted herewith, and readily conclude that the methods, devices, and controllers, as claimed in the Present Application were conceived prior to 27 June 2002, the filing date of the Barth patent publication.

6. In support of this conclusion, I have attached Exhibit A, which represents a redacted invention proposal disclosure document entitled "Multiplexing schemes for double data rate serial ATA PHY interface for PC mother chipset" ("Invention Proposal Disclosure") and Exhibit B which is a copy of the provisional patent application 60/409,367. Although the dates have been removed from the enclosed Invention Proposal Disclosure, I represent that this document represents conception of the invention at least prior to 27 June 2002.

7. In particular, a comparison between the figures of the Present Application, the figures of the Provisional Application, and the figures of the Invention Proposal Disclosure illustrate that Figures 1, 3, 4, 5C, 8, 9C, and 11 in the Present Application correspond closely to Figures 1, 3, 4, 5, 8, 9, and 11 of the Invention Proposal disclosure. Figures 7 and 10 in the present application are similar to the same Figures in the Disclosure, and Figure 14 in the present application is similar to Figure 2 in the invention proposal disclosure. Figures 1, 3, 4, 5, 7, 8, 9, 10, and 11 are the same or similar as between the provisional application and the invention proposal disclosure.

8. After conceiving this invention, I diligently proceeded to constructively reduce this invention to practice by participating in patent preparation activities and other aspects relating to preparation of the above-referenced Present Application with attorneys of Perkins Coie LLP.

9. I constructively reduced this invention to practice first with the filing of U.S. Provisional Patent Application 60/409,367 filed 06 September 2002 and then with the filing of U. S. Utility Patent application 10/658,590 on 08 September 2003, for which this affidavit is submitted, and each of which were based on the Invention Proposal Disclosure attached in Exhibit A.

10. I further declare that all statements herein made of my own knowledge are true and that all statements made on information or belief are believed to be

true; and further, that the statements are made with the knowledge that the making of willful or false statements or the like is punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and may jeopardize the validity of any patent issuing from the present patent application.

11. Signature

Ook Kim

Feb 26, 2009

Date

Residence: Palo Alto, California, USA

Citizenship: Korean

P.O. Address: 3145 Emerson Street, Palo Alto, CA 94306:

Enclosures:

Exhibit A – Invention Proposal Disclosure
Exhibit B – Provisional Patent Application 60/409,367

DECLARATION OF PRIOR INVENTION BY
OOK KIM UNDER 37 CFR § 1.131

EXHIBIT A

Silicon Image, Inc.

Invention Proposal

Inventor(s): Ook Kim, Robert Norman, Chi Wai Ho, Frank Lee, Dongyun Lee, Gijung Ahn, Seung Ho Hwang
Title: Multiplexing schemes for double data rate serial ATA PHY interface for PC mother chipset
Abstract: Serial ATA format is the serialized ATA format, which transfers data between CPU and HDD. In PC motherboard, there is a so-called chip set ASIC which interfaces CPU and various I/O. This ASIC controls various I/O and should have sufficient pin counts to support additional Serial ATA into the existing pin outs. This patent reveals how to add Serial ATA connection capability without increasing pin counts. Also, this scheme relieves high speed signaling burdens of chipset side ASIC. By multiplexing more than one SATA channels, it'll boost the maximum data transfer rate between CPU and HDD by allowing simultaneous communication for both master and slave HDDs. Additional calibration scheme generates optimum latching clocks, which relieves high speed I/O design problem in the motherboard chipset side.
Other Silicon Image staff familiar with the subject matter: Yeshik Shin, Kyutaeg Oh
Related prior art:

Inventor(s): Ook Kim, Robert Norman, Chi Wai Ho, Frank Lee, Dongyun Lee, Gijung Ahn, Seung Ho Hwang

_____ Date: [redacted]

Witness: Badar Bangal Date: _____

Detailed description of invention:

Serial ATA format is the serialized ATA format, which transfers data between CPU and HDD. In PC motherboard, there is a so-called chipset ASIC which interfaces CPU and various I/O. This ASIC controls various I/O and should have sufficient pin counts to support additional Serial ATA into the existing pin outs. This patent reveals how to add Serial ATA connection capability without increasing pin counts. Also, this scheme greatly relieves high speed signaling burdens from ASIC side.

Figure 1 shows the ATA HDD connection within PC system. In this case, the motherboard chip, so called south bridge, controls various I/O devices. ATA usually controls up to 2 devices per bus, which is normally 40-pin ribbon cable. This legacy ATA connection started from the early stage of PC development. As demands for higher capacity and higher speed between motherboard and peripheral HDD increases, newer standards developed to handler this request.

However, the Ribbon cable is still rather bulky and low in performance. As system integrates down to highly integrated level, the wide bus connection actually lies as a big barrier for better system improvements. There are several standards can be used for high speed data transport by serializing the data. By using high speed serial data transport signaling scheme, the number of required wires can be decreased down to minimum level, such as two pairs of differential high speed signals. SATA is the technology to exploit those innovations accrued into current high speed, low power CMOS technology to make it possible to build a very low cost serial link for PC motherboard application. But, it can be used for such as RAID or other mass storage devices.

From the user perspective point of view, it is highly desirable to support both of legacy ATA and serial ATA without increasing chipset complexity significantly and pin counts. Also, it is desirable that user can program whether to use SATA or legacy ATA. SATA alone can be used with only 4+α pins per channel. However, current chipset cannot easily implement SATA port into their ASIC, because those pins are rather sophisticated and involved with ultra high speed signaling and very low noise PLL and clock and data recovery schemes. Therefore, the invention describes the way how these links can be accomplished without increasing the design complexity and pin counts of chipset significantly.

The SATA can be divided into two major blocks as shown in figure 2. PHY mainly transforms parallel Tx data in digital signal level into serial Tx signals. Also PHY transforms serial data into parallel Rx data. Link mainly interfaces ATA protocol and SATA protocols.

SATA PHY can be configured as an interface between chipset and SATA serial data as shown in figure 3. In this case, the chipset has a built-in MUX to control the data stream, which is used either for ATA interface or for SATA interface. For ATA interface, the internal MUX operates in a very high speed and there would be very little effect on ATA operation. In SATA interface, it uses the same ports to communicate with PHY. However, in this case, the interface is no longer ATA interface signaling scheme.

Figure 4 shows one another configuration where SATA PHY both handles ATA interface and SATA interface. All ATA interfaces are buffered by this ASIC.

SATA schemes are composed of several critical signals. The interface will be synchronous between Tx and Rx. The asynchronous nature of ATA interface Rx and Tx can be handled by SATA PHY chip. The detailed implementation of this signaling can be shown in figure 5. Tx block in LINK transmits data latched by flip flop shown in figure 6. As long as the TBC clock is generated by the same D-FF, the data and clock are aligned with each other. This clock is send to PHY. PHY has a built-in PLL which detects transmit clock edge and extracts optimum edge TXCLK' as shown in figure 5 for latching. The conceptual diagram is shown in figure 6. With this scheme, two channel data can be also sent in a single ATA bus as well. With the high duration of the clock, data 'A' are sent and with the low duration of the clock, data 'B' are sent. PHY block has a built-in PLL which is used for transmitting low jitter, high speed serial data, this PLL can also be used for extracting the optimum clock phases for TXD data latching point.

For the receiving portion of the data, two clock signals are generated to latch incoming data. RBC0 is used for extracting 'A' block data and RBC1 is used for extracting 'B' block data. This relationship is shown in figure 7.

Inventor(s): Ook Kim, Robert Norman, Chi Wai Ho, Frank Lee, Donavun Lee, Gilung Ahn, Seung Ho Hwang

_____ Date: [redacted]

Witness: Badar Bagai _____ Date: _____

By using this scheme, 2 channels of SATA data can be sent on a single data lines. For generation 1 case defined in SATA specification, 150 Mbytes/sec data is transferred from LINK to PHY. By using double data rate transmission, 300 Mbytes/sec total data speed is achieved. For generation 2 case, total 600 Mbytes/sec total data speed is also achieved by having two 300 Mbytes/sec data channels in the link. Even though the chipset cannot deliver 600 Mbytes/sec for general case, it can transmit data within such condition as short distance and minimum capacitance loading. Also, by having calibration phases during setup link time, test pattern can be transmitted and PHY detects channel skew between clocks and data. By having high speed data input port for this link in PHY block, reliable transmission can be achieved by using moderate data and clock driver in the chipset.

In the RXD section, two clock signals such as RBC0 and RBC1 are generated from the PHY as shown figure 8. These two clock line signals both channel A and channel B. As link speed becomes higher, the optimum latching point for the RXD is very important to make a solid link between PHY and LINK. To make it further robust over various operation conditions and PCB traces, a calibration scheme can be used. Figure 9 shows the clock relationship in the calibration phases. RBC0,1 is moved relative to the RXD in the calibration phase. In this mode, LINK re-transmits received data through TX channel. By using adequate calibration test patterns generated by the PHY, PHY can detect the optimum RBC0,1 and RXD data relationship. It can also detects channel skews between RBC0,1. The start and end of calibration can be user operated such as shown in figure 10. However, some signals such as one bit of RXD or other signal bits can be used for this purpose as well.

There exists other control signals required between PHY and LINK as shown in CTRL1 and CTRL2 in figure 2. These signal can be various signals as follows

- COMMA : signals the detection of K28.5 signal defined 8B10B coding, PHY to LINK
- PARTIAL/SLUMBER : signals partial/slumber states, LINK to PHY
- CLOCK : main system clock, PHY to LINK
- COMINIT/COMWAKE : OOB (out of band) signaling
- RESET : SATA related RESET
- DATA_READY : For handshaking purpose
- TX_DATA_EN : For sending OOB data in Tx, LINK to PHY
- Other signals : status report between PHY and LINK

For each channel of SATA devices, those signals can also be multiplexed by using the scheme shown in the disclosure. For example, DATA_RREADY signal is used for signaling whether the RX data is valid or not. By using this signal, the rate difference between Rx and Tx can be controlled and only one synchronous clock can be used for both Rx and Tx data. In SATA implementation, redundant ALIGN primitive is inserted. The PHY can either insert or delete these signals. Also, in order to make the deletion more simple, additional data signal named DATA_READY can be used for both channels. Figure 11 shows the multiplexed signaling scheme for DATA_READY.

For less frequency signals, it can be multiplexed by combining several consecutive bits. In this case, a synchronization pattern can be used to synchronize those signals. For example, by combining 4 bits, we can define signal activity as follows.

1111 : alignment pattern

0XYZ : X, Y, Z is allocated for each bits for signaling.

In this case, each normal word except for the alignment pattern starts with 0. X is used for the signal X, Y is used for signal Y and Z is used for signal Z. For example X is RESET, Y and PARTIAL and Z is SLUMBER.

0000 : RESET is low, PARTIAL is low and SLUMBER is low

Inventor(s): Gok Kim, Robert Norman, Chi Wai Ho, Frank Lee, Dongyun Lee, Giiung Ahn, Seung Ho Hwang

Date: [redacted]

Witness: Nader Bagal Date:

0001 : RESET is low, PARTIAL is low and SLUMBER is high

By using this methods, the total number of signals to be used for supporting 2 channel SATA PHY can be minimal. One example for the usage of pins is shown in table 1.

Table 1. Pin number usage

Name	Number of pins	Purpose
TxD	10	LINK to PHY 10-bit data
TBC	1	Transmit byte clock
RXD	10	PHY to LINK 10-bit data
RBC0, RBC1	2	PHY to LINK byte clock
CTRL1	1	LINK to PHY control signals
CTRL2	1	PHY to LINK control signals
DATA_READY	1	DATA_READY signals
Total	26	

However, by using unused coding byte of for 8B10B coding in the TXD and RXD, those CTRL1, CTRL2, DATA_READY can also be eliminated. Then the minimum set of data is only 25 pins. This will greatly reduce the overhead to implement both SATA channel and ATA channel in chipset.

In conventional ATA scheme, only one of master or slave can have the control of ATA bus. By allowing two simultaneous communications of data, this method can boost the transport speed between CPU and HDD by two times.

Claims

Claim 1) A system composed of a chipset which interfaces between CPU and ATA interface, wherein additional Serial ATA functional block and a MUX are integrated and an external Serial ATA chip which both transmits and receives high speed serial and the external SATA chip is connected to the ATA bus signals.

Claim 2) The MUX in claim 1, connects either connects ATA signaling or SATA signaling to the I/O block depending ATA mode or SATA mode.

Claim 3) The chipset may integrate more than one channel of Serial ATA and has a time division multiplexing scheme which uses both of multiple Serial ATA parallel data at the same data lines.

Claim 4) The external Serial ATA chip which serialize transmit parallel data and de-serialize the incoming serial data to receive parallel data may have more than one channel of Serial ATA and has an another time domain multiplexing and de-multiplexing circuitry.

Claim 5) A calibration scheme, which is first initiated by the internal SATA block which is integrated into chipset, sends the start of calibration signal to the external SATA block and the external SATA block starts to send calibration pulses to the data channel through receive data block. The internal SATA block loop backs the received data and the external SATA block detects the optimum relative position between the received byte clock and the received data to minimize communication errors.

Claim 6) Out of band signals which is not used in 8B10B coding space is used for signaling purpose between internal SATA block and external SATA block.

Claim 7) Additional control signal lines are multiplexed to a less number of lines by using time domain multiplexing.

Claim 8) The MUX in claim 1, either operates as one channel SATA I/O or as a multiple channel by using duplex mode in time domain.

Inventor(s): Ook Kim, Robert Norman, Chi Wai Ho, Frank Lee, Dongyun Lee, Gihung Ahn, Seung Ho Hwang

Date: [redacted]

Witness: Badar Bagal Date:

Claim 9) The PHY in claim 1, can have a ATA compliant 5-V tolerant I/O works as a buffer between the chipset and ATA devices in ATA mode. This makes it possible for the chipset to handle only low voltage digital I/O and the external PHY handles 5-V tolerant high frequency signaling.

Inventor(s): Ook Kim, Robert Norman, Chi Wai Ho, Frank Lee, Dongyun Lee, Chiuna Ahn, Seung Ho Hwang

Date: [redacted]

Witness: Bedar Hagai Date:

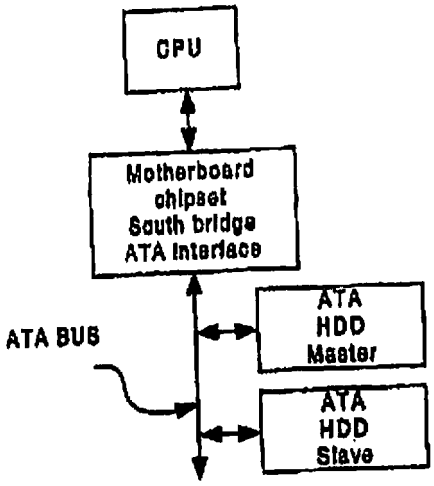

Figure 1. ATA HDD connection schemes in the conventional PC systems

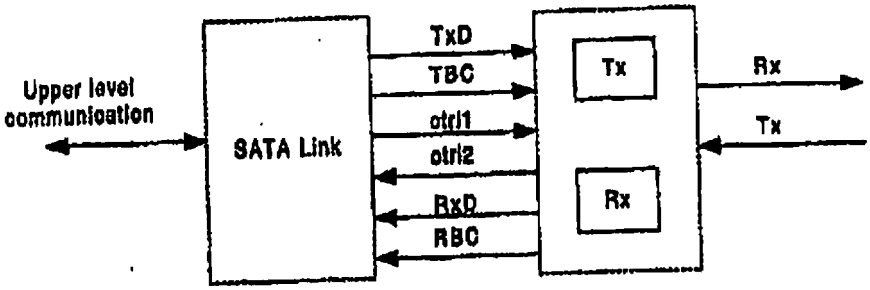

Figure 2. SATA block diagram

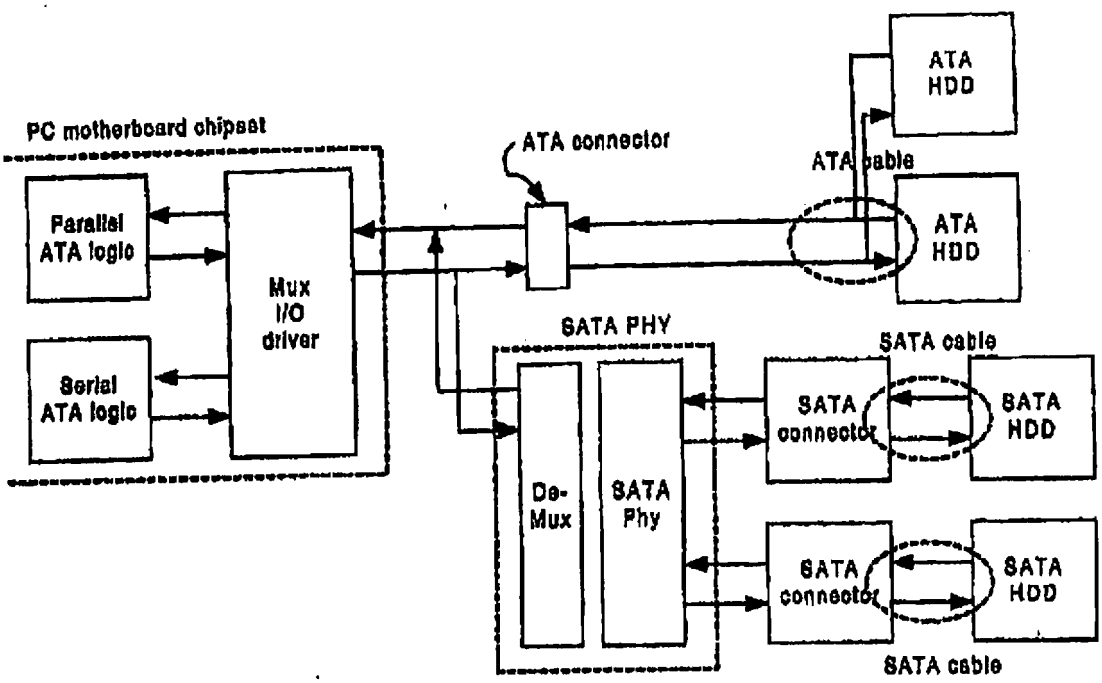

Figure 3. SATA and ATA configuration

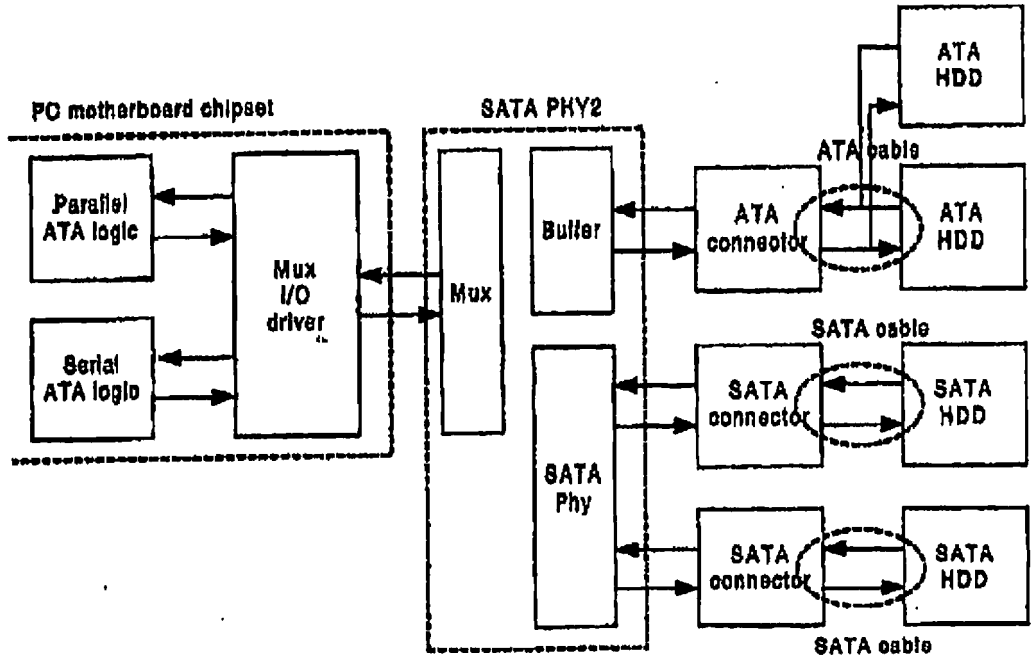

Figure 4. SATA PHY2 configuration

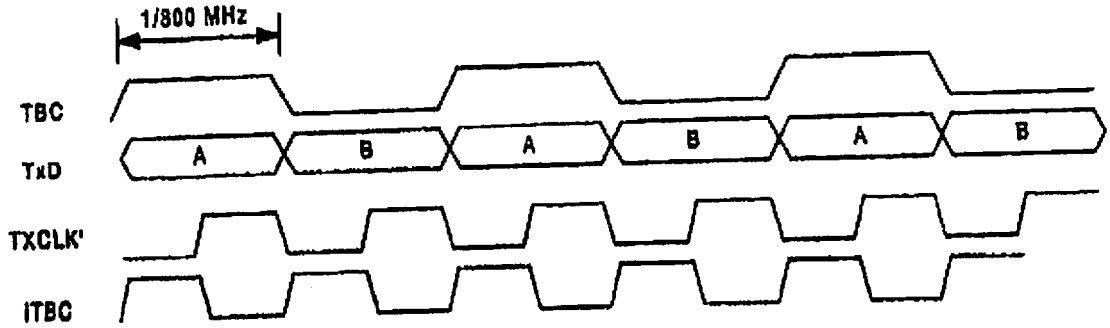

Figure 5. TxD and TBC timing diagram

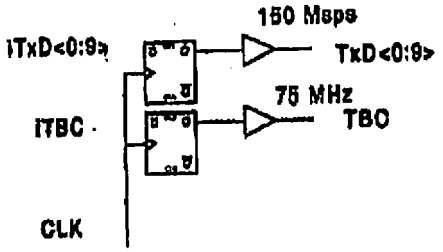

Figure 6. TxD and TBC generation

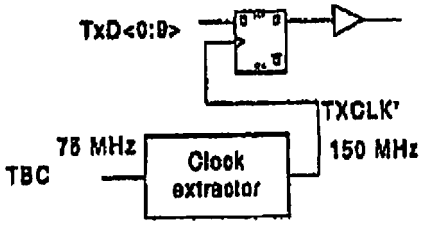

Figure 7. PHY portion of TBC and TxD block

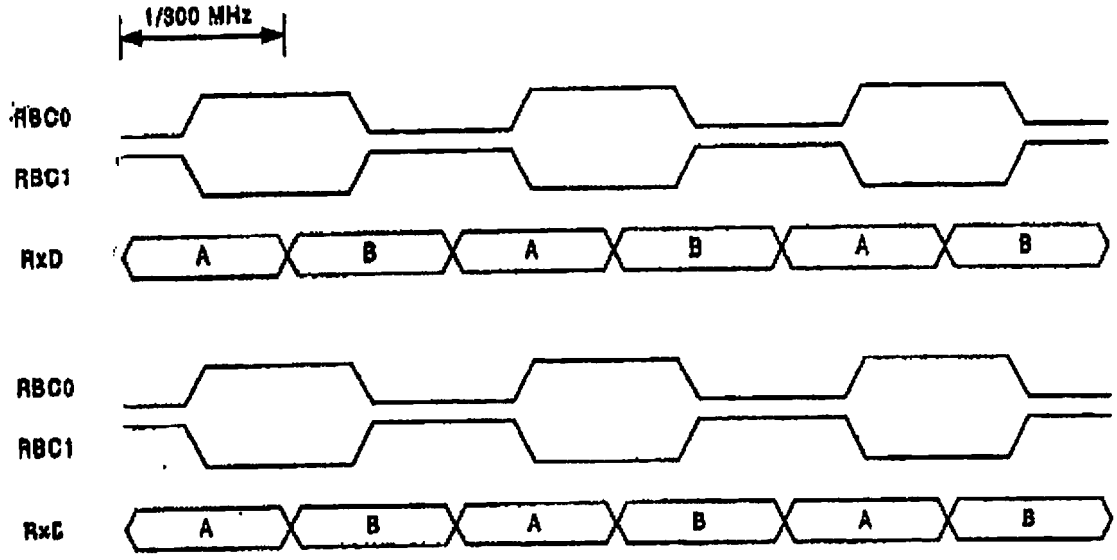

Figure 8. The timing diagram of RBC0, RBC1 and RxD

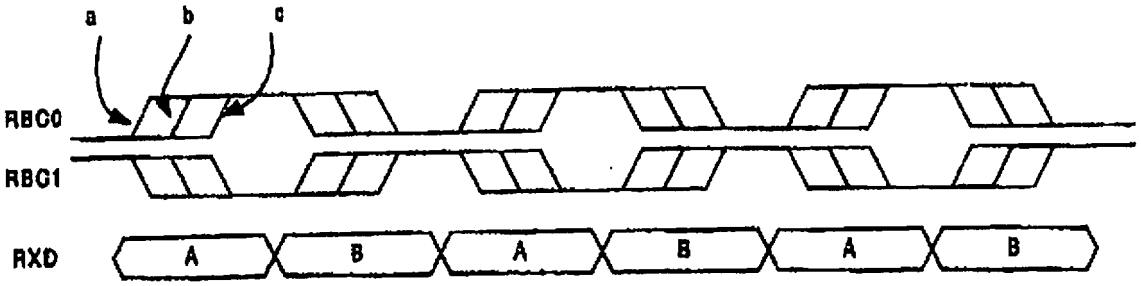

Figure 9. various RBC0, RBC1 timing relationships in RXD, RBC calibration phases

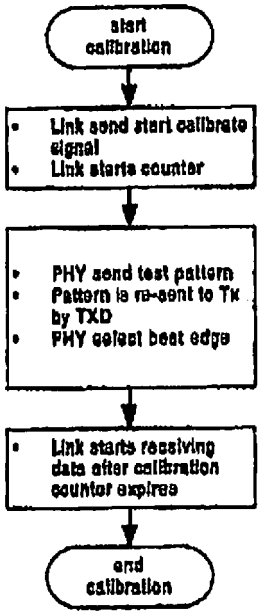

Figure 10. Algorithms of RBC calibration

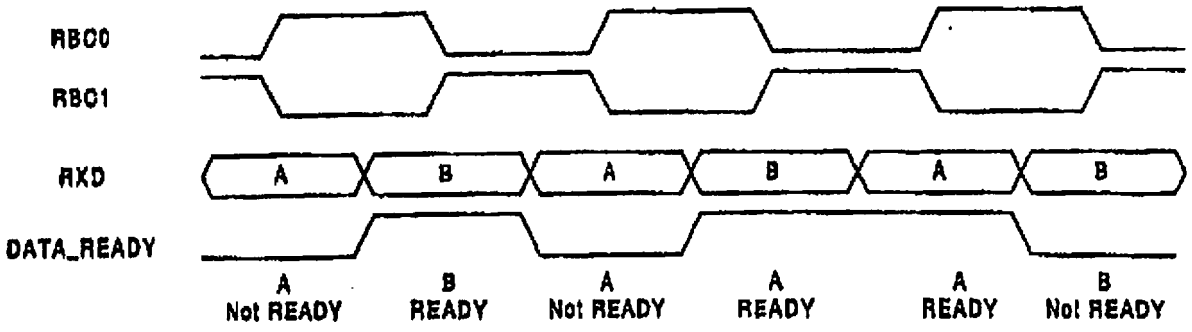

Figure 11. DATA_READY signal multiplexing schemes

DECLARATION OF PRIOR INVENTION BY
OOK KIM UNDER 37 CFR § 1.131

EXHIBIT B

METHODS AND APPARATUS FOR DOUBLE DATA RATE SERIAL ATA PHY INTERFACE

by Inventor

Ook Kim

FIELD OF THE INVENTION

The present invention relates computer cable connectors and more particularly to hard disk drive (HDD) cable connectors.

BACKGROUND OF THE INVENTION

ATA (advanced technology attachment or AT attachment – a reference to AT/286 computers) has been the standard internal storage interconnect for desktop and mobile computers since the 1980's. ATA's relative simplicity, low cost and high performance has enabled it to remain in use for an extended period of time.

Despite these advantages, a number of limitations exist. ATA uses a 5-volt signal requirement. Use of this standard is becoming incompatible with cutting edge integrated circuits that are designed to operate at a lower voltage. Also, ATA requires a high pin count which necessitates a bulky ribbon cable. The high pin count is problematic for chip design and the ribbon cable impedes airflow which makes thermal design difficult. Finally, ATA data transfer rate is limited to about 100 megabytes/second maximum.

Due to those limitations, a new standard has been defined for the next generation ATA. This standard is called serial ATA or SATA for short. This new standard allows for data transfer speeds starting at 150 megabytes/second and ultimately up to 600 megabytes per second. Advantageously, it also employs a much thinner cable with a smaller pin count.

As the new SATA standard gains widespread use, undoubtedly there will be computer users who may wish to use both older style ATA Hard Disk Drives (HDDs) and SATA HDDs in one system. Figure 1 illustrates a prior art computer system **10** that employs ATA style HDDs. Included in the system is a CPU **20**, a motherboard chipset or South Bridge **30**, an ATA bus **40**, a first ATA HDD **50** and a second ATA HDD **60**. In the ATA configuration, only one ATA bus is used and only 1 HDD can communicate to the CPU at a time.

Figure 2 shows a computer system **70** that uses the newer SATA configuration. Similar to the ATA setup, there is a CPU **20** and a South Bridge interface **30**. Also included is a first SATA HDD **80** and a second HDD SATA **90**. Unlike the ATA configuration, each SATA HDD **80** and **90** are connected directly to the South Bridge via separate SATA links **90** and **100**.

It is readily recognized that, in the prior art, in order to use both style connectors in one system, more cables would need to be added or the SATA and ATA type connectors would need to be combined into one larger, more complex, more expensive and unwieldy cable.

Accordingly, what is needed is a way easily connect an SATA HDD into an existing system containing ATA HDD's without having to add more cables or add to the pin count of the existing ATA connector.

SUMMARY OF THE INVENTION

The present invention provides a method and apparatus for adding a SATA HDD into an existing system containing ATA HDDs without having to add more cables or add to the pin count of the existing ATA connector.

One system of the present invention includes an apparatus or system including a chipset which interfaces between a CPU and an ATA interface. Additional SERIAL ATA functional blocks and a MUX are integrated into the chipset. An external SERIAL ATA chip that both transmits and receives high speed serial and the external SATA chip is connected to the ATA bus signals. The present invention therefore supports a mixture of HDD drive types without adding additional cables or increasing the pin count of an existing ATA connector.

A method of operating in ATA and SATA modes, in accordance with an embodiment of the present invention, includes selecting an ATA mode of operation. A first set of bi-directional signals compatible for communicating with an ATA HDD is multiplexed. An SATA mode of operation is selected and a second set of bi-directional signals compatible for communicating with an SATA HDD is then multiplexed.

These and other advantages of the present invention will become apparent to those skilled in the art after reading the following descriptions and studying the various figures of the drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a partial block diagram of a prior art computer system that employs ATA style HDD's.

Figure 2 is a partial block diagram of a computer system that employs SATA style HDDs.

Figure 3 is a partial block diagram of a computer system that utilizes both ATA and SATA style HDDs, in accordance with an embodiment of the present invention.

Figure 4 is a partial block diagram of a computer system that utilizes both ATA and SATA style HDDs, in accordance with another embodiment of the present invention.

Figure 5 is a timing diagram for TxD and TBC, in accordance with the present invention.

Figure 6 is a schematic of a circuit which generates TxD and TBC for a multiplexer, in accordance with the present invention.

Figure 7 is a block diagram of the PHY portion of the TBC and the TxD block, in accordance with the present invention.

Figure 8 is a timing diagram of RBC0, RBC1 and RxD, in accordance with the present invention.

Figure 9 is a timing diagram of RBC0 and RBC1 timing relationships in RXD and RBC calibration phases, in accordance with the present invention.

Figure 10 is a flow chart for RBC calibration, in accordance with the present invention.

DETAILED DESCRIPTION OF THE INVENTION

Figs. 1-2 were previously described with reference to the prior art.

SATA PHY can be configured as an interface between a chipset and an SATA serial data as shown in figure 3. In this case, the chipset has a built-in MUX to control the data stream, which is used either for the ATA interface or for the SATA interface. For the ATA interface, the internal MUX operates at a very high speed and there is very little effect on the ATA operation. In the SATA interface, it uses the same ports to communicate with PHY. However, in this case, the interface is no longer employing the ATA interface signaling scheme.

Figure 4 shows one other configuration where SATA PHY both handles ATA interface and SATA interface. All ATA interfaces are buffered by this ASIC. SATA schemes are composed of several critical signals. The interface will be synchronous between TX and Rx. The asynchronous nature of ATA interface Rx and Tx can be handled by SATA PHY chip. The detailed implementation of this signaling can be shown in figure 5. Tx block in LINK transmits data latched by flip flop shown in figure 6. As long as the TBC clock is generated by the same D-FF, the data clock are aligned with each other. This clock is sent to PHY. PHY has a built-in PLL which detects transmit clock edge and extracts optimum edge TXCLK' as shown in figure 5 for latching. The conceptual diagram is shown in figure 6. With this scheme, two channel data can be also sent in a single ATA bus as well. With the high duration of the clock, data 'A' is sent and with the low duration of the clock, data 'B' is sent. PHY block has a built-in PLL which is used for transmitting low jitter, high speed serial data, this PLL can also be used for extracting the optimum clock phases for TXD data latching point.

For the receiving portion of the data, two clock signals are generated to latch incoming data. RBC0 is used for extracting 'A' block data dn RBC1 is used for extracting 'B' block data. This relationship is shown in figure 7.

By using this scheme, 2 channels of SATA data can be sent on a single data line. For the generation 1 case defined in SATA specification, 150 Mbytes/sec data is transferred from LINK to PHY, by using double data rate transmission, 300 Mbytes/sec total data speed is achieved. For the generation 2 case, total 600 Mbytes/sec total data speed is also achieved by having two 300 Mbytes/sec data channels in the link. Even though the chipset cannot deliver 600 Mbytes/sec for general case, it can transmit data within such condition as short distance and minimum capacitance loading. Also, by having calibration phases during setup link time, test patterns can be transmitted and PHY detects channel skew between clocks and data. By having high speed data input port for this link in the PHY block, reliable transmission can be achieved by using moderate data and clock driver in the chipset.

In the RXD section, two clock signals such as RBC0 and RBC1 are generated from the PHY as shown in figure 8. These two clock lines signals are both channel A and channel B. As the link speed becomes higher, the optimum latching point for the RXD is very important to make a solid link between PHY and LINK. To make it more robust over various operation conditions and PCB traces, a calibration scheme can be used. Figure 9 shows the clock relationship in the calibration phases. RBC0,1 is moved relative to the RXD in the calibration phase. In this mode, LINK re-transmits received data through TX channel. By using adequate calibration test patterns, generated by the PHY, PHY can detect the optimum RBC0,1 and RXD data relationship. It can also detect channel skews

between RBC0,1. The start and end of calibration can be timer operated such as shown in figure 10. However, some signals such as one bit of RXD or other signal bits can be used for this purpose as well.

Other control signals are also required between PHY and LINK as shown in CTRL1 and CTRL2 in figure 2. These signals can be various signals as follows:

- COMMA : signals the detection of K28.5 signal defined 8B10B coding, PHY to LINK
- PARTIAL/SLUMBER : signals partial/slumber states, LINK to PHY
- CLOCK : main system clock, PHY to LINK
- COMINIT/COMWAKE : 00B (out of band) signaling
- REST : SATA related RESET
- DAZATA READY : For handshaking purposes
- TX_DATA_BN : For sending OOB data in Tx, LINK to PHY
- Other signals : status report between PHY and LINK

For each channel of SATA devices, those signals can also be multiplexed by using the scheme shown in the disclosure. For example, DATA_READY signal is used for signaling whether the RX data is valid or noting this signal, the rate difference between RX and Tx can be controlled and only one synchronous clock can be used for both Rx and Tx data. In the SATA implementation, a redundant ALIGN primitive is inserted. The PHY can either insert or delete these signals. Also, in order to make the deletion more simple, an additional data signal named DATA_READY can be used for both channels. Figure 11 shows the multiplexed signaling scheme for DATA_READY.

For less frequency signals, it can be multiplexed by combining several consecutive bits. In this case, a synchronization pattern can be used to synchronize those signals. For example, by combining 4 bits, we can define signal activity as follows:

1111 : alignment pattern

OXYZ : X, Y, Z is allocated for each bits for signaling.

In this case, each normal word except for the alignment pattern starts with o. X is used for the signal X, y is used for signal Y and Z is used for signal Z. For example X is RESET, Y and PARTIAL and Z is SLUMBER.

0000: RESET is low, PARTIAL is low and SLUMBER is low

0001 : RESET is low, PARTIAL is low and SLUMBER is high

By using these methods, the total number of signals to be used for supporting 2 channel SATA PHY can be minimized. One example for the usage of pins is shown in table 1.

Table 1. Pin number usage

Name	Number of pins	Purpose
TxD	10	LINK to PHY 10-bit data
TBC	1	Transmit byte clock
RXD	10	PHY to LINK 10-bit data
RBC0, RBC1	2	PHY to LINK byte clock
CTRL1	1	LINK to PHY control signals
CTRL2	1	PHY to LINK control signals
DATA_READY	1	DATA_READY signals
Total	26	

However, by using unused coding bytes for 8B10B coding in the TXD and RXD, those CTRL1, CTRL2 and DATA_READY can also be implemented. Then the minimum set of data is only 25 pins. This will greatly reduce the overhead to implement both SATA channel and ATA channels in a chipset.

In the conventional ATA scheme, only one of the master or slave can have control of the ATA bus. By allowing two simultaneous communications of data, this method can boost the transport speed between the CPU and the HDD by a factor of two.

While this invention has been described in terms certain preferred embodiments, it will be appreciated by those skilled in the art that certain modifications, permutations and equivalents thereof are within the inventive scope of the present invention.

CLAIMS

1. A system comprising a chipset which interfaces between CPU and ATA interface, wherein additional Serial ATA functional block and a MUX are integrated and an external Serial ATA chip which both transmits and receives high speed serial and the external SATA chip is connected to the ATA bus signals.

2. The MUX in claim 1, connects either ATA signaling or SATA signaling to the I/O block depending on the ATA mode or the SATA mode.

3. The chipset may integrate more than one channel of Serial ATA and has a time division multiplexing scheme which uses both of multiple Serial ATA parallel data at the same data lines.

4. The external Serial ATA chip which serialize transmit parallel data and de-serialize the incoming serial data to receive parallel data may have more than one channel of Serial ATA and has another time domain multiplexing and de-multiplexing circuitry.

5. A calibration method, which is first initiated by the internal SATA block which is integrated into the chipset, sends the start of a calibration signal to the external SATA block and the external SATA block starts to send calibration pulses to the data channel through the receive data block. The internal SATA block loop backs the received data and the external SATA block detects the optimum relative position between the received byte clock and the received data to minimize communication errors.

6. Out of band signals which is not used in 8B10B coding space is used for signaling purposes between an internal SATA block and an external SATA block.

7. Additional control signal lines are multiplexed to a lesser number of lines by using time domain multiplexing.

8. The MUX in claim 1, either operates as one channel SATA I/O or as a multiple channel by using a duplex mode in the time domain.

9. The PHY in claim 1, either operates as one channel SATA I/O or as a multiple channel by using duplex mode in the time domain.

10. A method of operating in ATA and SATA modes comprising:

selecting an ATA mode of operation;

multiplexing a first set of bi-directional signals compatible for communicating with an ATA HDD;

selecting an SATA mode of operation; and

multiplexing a second set of bi-directional signals compatible for communicating with an SATA HDD.

MULTIPLEXING SCHEMES FOR DOUBLE DATA RATE SERIAL ATA PHY INTERFACE FOR PC MOTHER CHIPSET

ABSTRACT OF THE DISCLOSURE

A system composed of a chipset which interfaces between a CPU and an ATA interface wherein additional SERIAL ATA functional blocks and a MUX are integrated and an external SERIAL ATA chip that both transmits and receives high speed serial and the external SATA chip is connected to the ATA bus signals. This permits a mixture of hard disk drive (HDD) types to be supported, such as ATA HDDs and SATA HDDs, without requiring extra cabling or adding to the connector pin count.

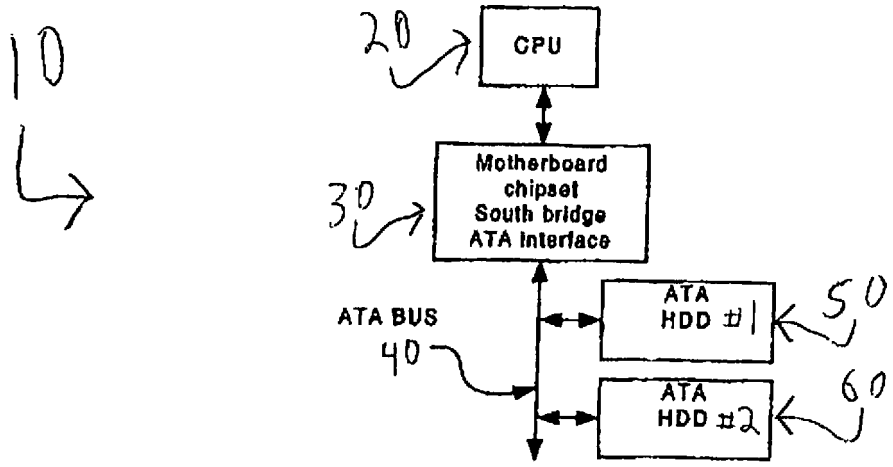

FIGURE 1
(PRIOR ART)

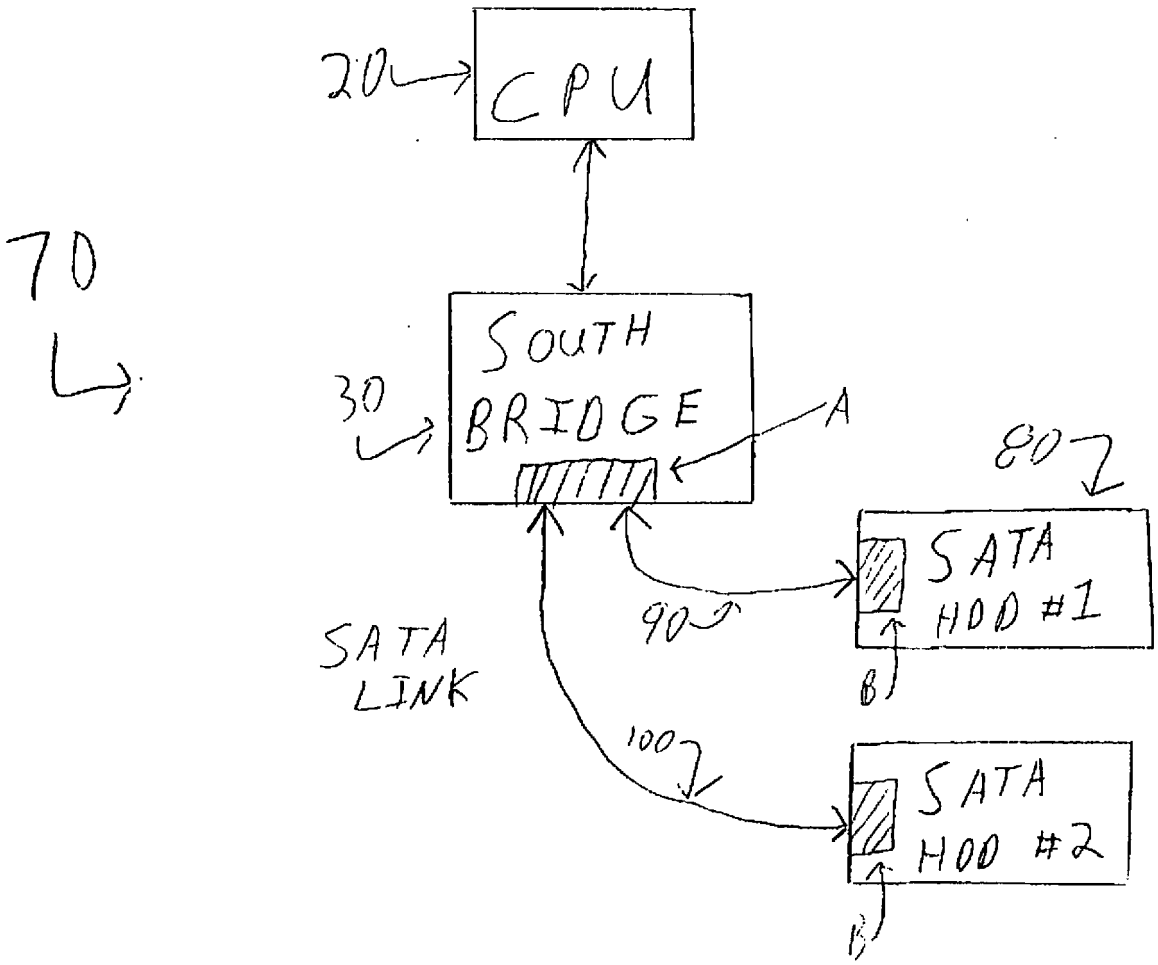

FIGURE 2
SATA LINKED SYSTEM
(PRIOR ART)

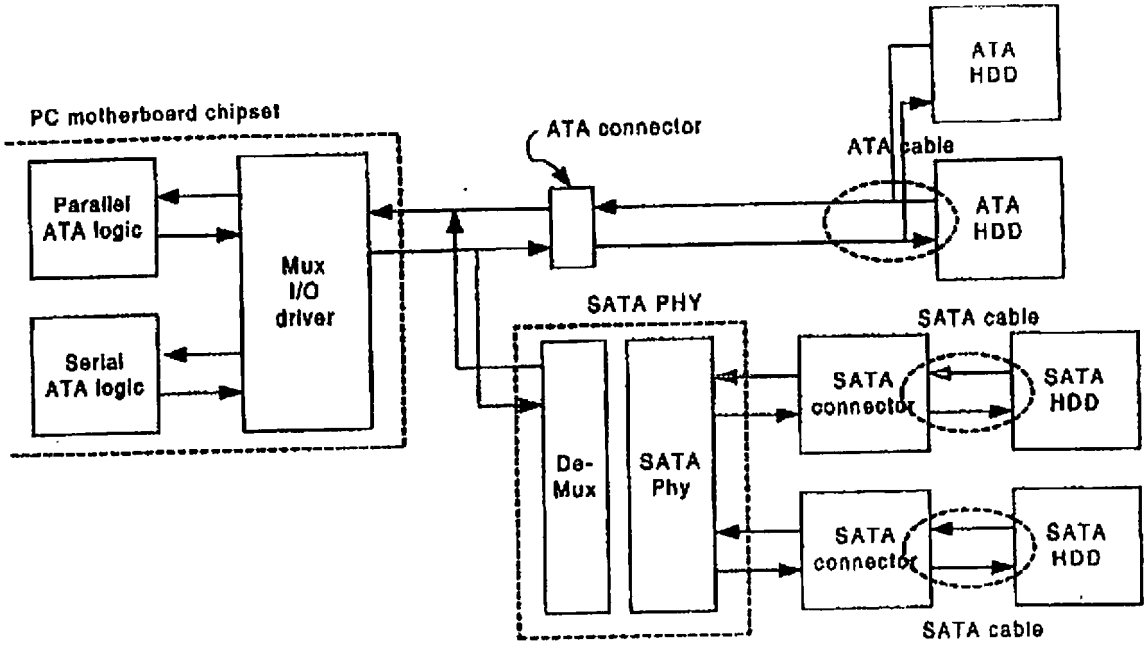

Figure 3. SATA and ATA configuration

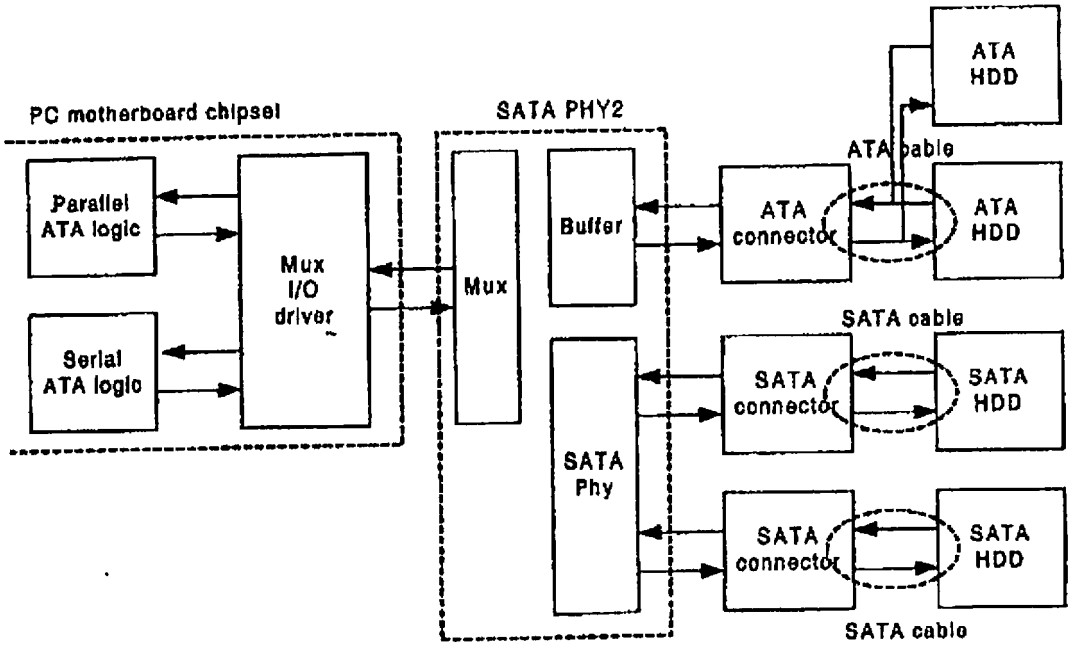

Figure 4. SATA PHY2 configuration

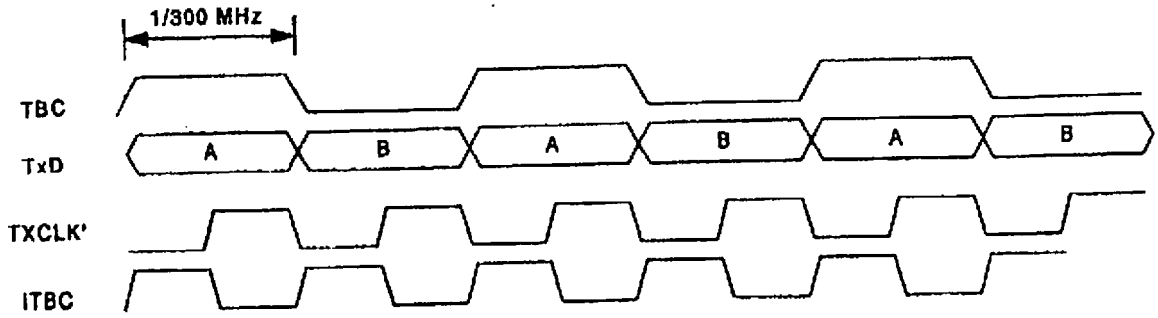

Figure 5. TxD and TBC timing diagram

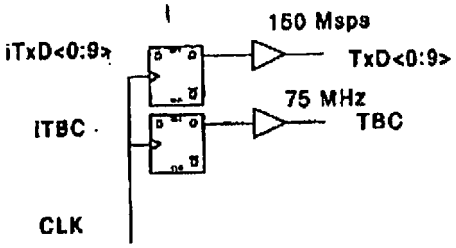

Figure 6. TxD and TBC generation

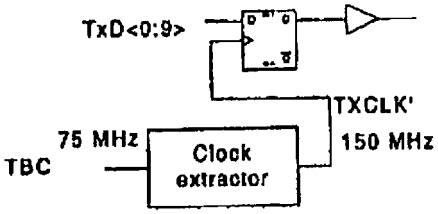

Figure 7. PHY portion of TBC and TxD block

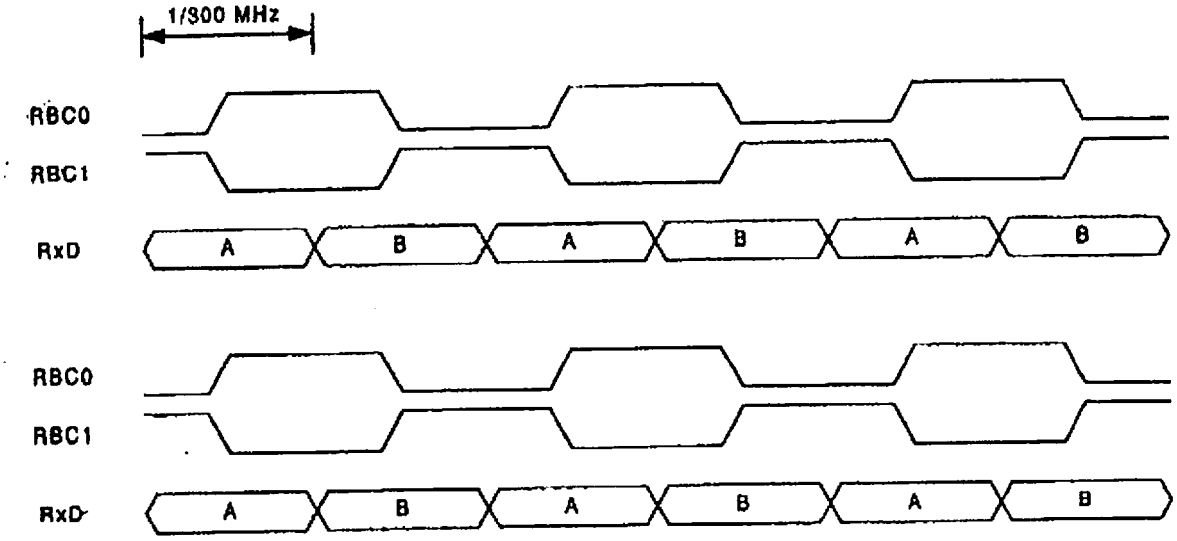

Figure 8. The timing diagram of RBC0, RBC1 and RxD

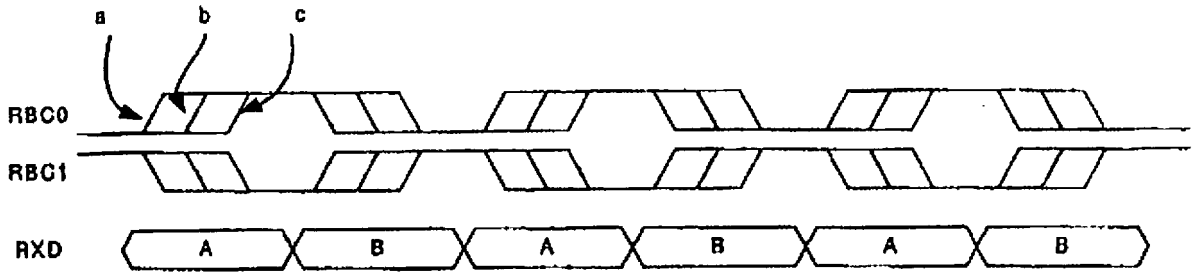

Figure 9. various RBC0, RBC1 timing relationships in RXD, RBC calibration phases

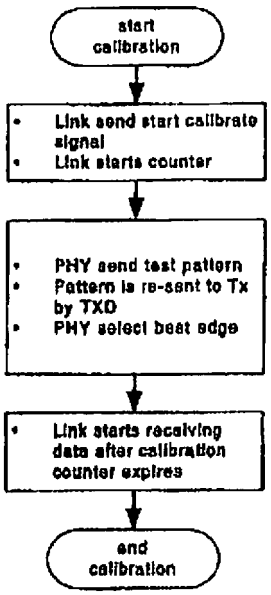

Figure 10. Algorithms of RBC calibration

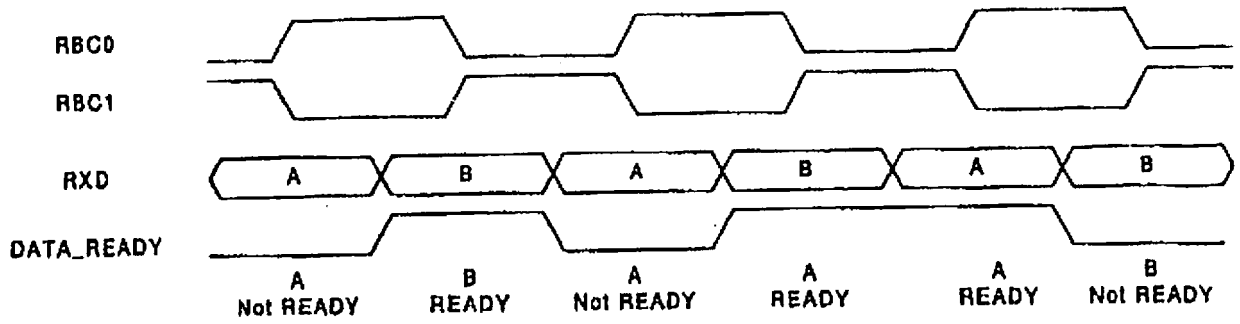

Figure 11. DATA_READY signal multiplexing schemes